

11/16/98
JCS49 U.S. PTO

PATENT
Docket No. Fuehrer 2-9-24-11

Express Mail No. EL162687936US

A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JCS49 U.S. PTO
09/192651

11/16/98

INVENTORS: T.E. Fuehrer
 K.E. Hollenbach
 D.R. Laturell
 S.B. Witmer

APPLICATION NO. Not Yet Assigned

FILED: Herewith

TITLE: COMBINATION CLOCK AND CHARGE
 PUMP FOR LINE POWERED DAA

* * * * * * * * * * * * *

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this correspondence, along with any papers indicated as being enclosed, are being deposited as Express Mail, (label EL162687936US), postage prepaid, in an envelope addressed to: Box Patent Application, The Assistant Commissioner for Patents, Washington, D.C. 20231, on November 16, 1998.

November 16, 1998

Date

Mamie Dedmon

Mamie Dedmon

* * * * * * * * * * * * *
BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

NEW APPLICATION TRANSMITTAL LETTER

Sir:

Enclosed are the following papers relating to the above-named new application for patent:

1. Specification (14 pgs., including claims and abstract);
2. Drawings (2 sheets) - informal;
3. Combined Declaration and Power of Attorney executed by Timothy Fuehrer, Keith Hollenbach, Donald Laturell and Steven Witmer executed on November 5, 1998; and

4. An Assignment and Agreement (with cover sheet) executed by Timothy Fuehrer, Keith Hollenbach, Donald Laturell and Steven Witmer executed on November 5, 1998.

CLAIMS AS FILED				
	No. Filed	No. Extra	Rate	Calculations
Total Claims	13 - 20 =	0	\$22	\$0.00
Independent Claims	3 - 3 =	0	\$82	\$0.00
Multiple Dependent Claim(s), if applicable			\$270 =	\$0
Basic Filing Fee				\$790.00
			Total Fee:	\$790.00

Please file the application and charge Lucent Technologies' Deposit Account No. 12-2325 the amount of \$790 to cover the filing fee. Two copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Deposit Account No. 12-2325 as required to correct the error.

Please address all correspondence to:

Mark D. Simpson
Synnestvedt & Lechner
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107-2950

Telephone calls should be directed to the undersigned at (215) 923-4466.

Respectfully submitted,

11/16/98
Date



Mark D. Simpson
Registration No. 32,942
Attorney for Applicants
Lucent Technologies Inc.
600 Mountain Avenue
P.O. Box 636
Murray Hill, New Jersey 07974-0636

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**COMBINATION CLOCK AND
CHARGE PUMP FOR LINE POWERED DAA**

Inventors: **T.E. Fuehrer**
 K.E. Hollenbach
 D.R. Laturell
 S.B. Witmer

Assignee: LUCENT TECHNOLOGIES, INC.

Lucent Managing Attorney: John P. Veschi

Mark D. Simpson, Esquire
Registration No. 32,942
Synnestvedt & Lechner
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107

Telephone: (215) 923-4466
Facsimile: (215) 923-2189
E-mail: synnlech@synnlech.com

(S&L Docket No. P22,444 USA)

**COMBINATION CLOCK AND
CHARGE PUMP FOR LINE POWERED DAA**

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to an application entitled "Line
5 Interface Circuit with Event Detection Signaling" and an
application entitled "Event Detection Circuit", both of which are
assigned to the assignee of the present invention and both of
which were filed concurrently with this application.

FIELD OF THE INVENTION

This invention relates generally to the field of
10 telecommunications networks, and more particularly, to a
differential capacitively coupled clock used as a charge pump to
provide power to a circuit during the on-hook state.

BACKGROUND OF THE INVENTION

Telephone networks comprise a series of interconnected
15 subsystems that are linked together at points called interfaces.
These interfaces provide a link between old and new equipment and
allow for simplified design and maintenance. A local loop is an
example of an interface that connects a subscriber's telephone
20 set and a central office.

The isolation between the line side (the side having a
direct connection to the central office) and the computer side
(the side having a direct connection to the user premises
equipment) is often accomplished within the interface circuit. A
25 modem is an example of an interface circuit that may include

09126554-14562

5 circuitry that provides electrical isolation from the line in addition to the signal modulation and demodulation function of the modem. Isolation transformers, optical coupling, and capacitive coupling are all examples of known methods of isolating the line side from the computer side.

Fig. 1 is a block diagram of a typical telecommunication system 5 showing the connection between a subscriber and a central office that controls the telecommunication system. Central-office equipment 10 on the line side 15 of the telecommunication system 5 is connected to user device 20 (e.g., telephones or computer terminals) on the computer side 25 of the telephone system 5 via an interface circuit 30.

The DC power inherent in a telephone line provides a convenient source of power, but there are often limitations and restrictions which limit the ability of a modem to derive power from the telephone line. For instance, present regulations in the United States require that significant current may only be drawn from the telephone line when the telephone or modem is in an off-hook or active condition.

The U.S. Federal Communication Commission (FCC) and other counterpart regulatory agencies in other countries also require electrical isolation between the line side and the user devices on the computer side. Electrical isolation protects the line side from damage transmitted from the computer side and vice-versa. Many components (e.g., data access arrangements (DAAs) or CODEC's) of telephone interface circuits are PSTN line-powered

circuits, i.e. they operate from PSTN line current because they are isolated from the low voltage power supplies. The DAA must provide isolation between the low-voltage computer side and the high-voltage line side. Because the line-powered interface 5 circuits are isolated from low voltage power supplies and the amount of line current available to operate the interface circuits is severely limited during the on hook state by PSTN regulations, the on-hook functions are difficult to perform without the use of expensive transformers and/or optocouplers.

10 When a circuit on the line side is placed in the "on-hook" state (e.g., a telephone receiver on the computer side is placed in its cradle) the local loop is opened and almost all of the power to the interface circuit is cut off. Activating the DAA or CODEC requires that some power be drawn from the local loop or 15 from another source.

While in the on-hook state a small amount of current (idle-state loop current or leakage current) can be drawn for a short period of time from the TIP/RING line to operate the DAA or CODEC. Typically, the maximum AC loop current that can be drawn 20 from the TIP/RING line is about $500\mu\text{A}$ DC during ringing and about $200\mu\text{A}$ during caller ID transmission. The maximum amount of leakage current allowed is only $7\mu\text{A}$ of DC current. Accordingly, complicated power management techniques have been implemented 25 which must be used so that the power for the DAA or CODEC is minimized and is allocated only when it is clear that the power is necessary. For example, systems have been developed that will

RECORDED IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

operate in a low power mode (e.g., 20 μ A) during a discrimination stage where a determination is made that a real event (as opposed to line noise which appears to be an event) has occurred, and then switch to a medium power mode (e.g., 50 μ A) during a transmission mode where the event data is transmitted across the capacitive interface. Since there is so little current available during the on-hook state, it is extremely difficult to power the required circuits needed to perform on-hook functions.

In view of the tight limitations relating to the drawing of power, it would be desirable to develop a power source that would not derive power from leakage current, idle-state loop current and that would instead utilize otherwise "discarded" power to isolated circuits.

SUMMARY OF THE INVENTION

The present invention is a method and apparatus which facilitates the use of existing power that is ordinarily unused or discarded to provide power to an interface during the on-hook state, thereby alleviating the need to use loop current to power the interface during the on-hook state. The present invention utilizes existing clock signals to charge capacitors that are normally used for capacitive coupling of digital data across the high voltage isolation barrier. Although only smaller capacitors are needed for transmitting data across the capacitive interface, larger capacitors are used and are configured to form a charge pump to generate power to the interface at all times. Thus the

interface always has a steady source of power available for use, including during the on-hook state, for powering circuitry that can detect, modulate, and transmit on-hook signals across the capacitive interface. The amount of current available to the interface from the charge pump is at least one milliamp or more, a dramatic increase over the typical $2\mu\text{A}$ of current that is only sporadically available from leakage current during the on-hook state.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a typical telecommunications system in which the present invention may be utilized;

Fig. 2 is a block diagram of the interface circuit of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

As described below in more detail and in accordance with an embodiment of the invention shown in Fig. 2, a network interface circuit 100 comprises a DSP 110 and a DAA 120 connected to a telephone line via a switch hook comprising transistors Q2 and Q4 and resistor R2. DSP 110 includes a differential driver 112 which provides a differential clock signal to the DAA 120.

Although the embodiment described with respect to Fig. 2 shows a DSP 110 connected to DAA 120, it is understood that any device having a driver circuit such as a clock generator could be utilized instead of a DSP, depending on the needs of the user.

For example, it is contemplated that a microprocessor, an ASIC, or a CPU could be used in place of the DSP to provide the means for developing a charge across the capacitive elements of the interface.

5 The DAA 120 includes a differential driver circuit 122, a Sigma-Delta analog-to-digital converter 124 and Caller ID and Ringing Preamplifier 126, all of which are coupled in series to the TIP/RING line via a capacitor C_{x1} . Capacitor C_{x1} couples the ringing and caller ID signal to the DAA during the on-hook state.

10 When the system is in the on-hook state, the switch hook of the telephone is open (Q2 not conducting) and line current is not available for use by the DAA. As described below, however, the DAA is powered by a charge pump 132 and thus does not need the line current to operate. Capacitor C_{x1} is optimally a 20 pF to 15 50 pF capacitor. When the switch hook is closed, current flows through transistors Q2 and Q1. The AC signal present during the off-hook state is also coupled in the DAA through a different path (not shown). Modem data is transmitted during the off-hook state but the current is pulled directly from the telephone line, 20 so the charge pump is not needed.

A charge pump 132 comprises a first capacitive element (charge pump capacitors C_{c1} and C_{c2}), a second capacitive element (external capacitor C_{ext}), and a rectifying element (diodes D1, D2, and D3). Also included in the DAA 120 is clock regeneration 25 circuit 130. The clock regeneration circuit 130 is preferable because the charge pump 132 distorts the driver waveform across

diode D3, shifting the DC level. By capacitively coupling the differential signal across diode D3, the DC signal is removed. The clock regeneration circuit then "regenerates" a new clean clock signal synchronized to the driver pulses. Capacitors C_{C3} and C_{C4} provide AC coupling for the clock regeneration circuit

5 130. Diodes D1, D2 and D3 rectify and double the clock signals for the purpose of charge pumping. External capacitor C_{EXT} stores energy for the DAA 120 transmitted across the charge pump capacitors C_{C1} and C_{C2} and rectified by diodes D1, D2, and D3.

10 The charge on capacitor C_{EXT} is replenished by the charge pump capacitors C_{C1} and C_{C2} . C_{EXT} enables the peak current pulled from the charge pump 132 to be larger than the average current supplied by the charge pump 132.

1 *all all all all all all all all all all*

15 Coupled between the DSP 110 and the DAA 120 are a series of capacitors C_{T1} , C_{T2} , C_{R1} , C_{R2} , in addition to charge pump capacitors C_{C1} , and C_{C2} . Capacitors C_{T1} and C_{T2} capacitively couple the transmit signal (a digital signal) to DAA 120 from the DSP 110. Capacitors C_{R1} and C_{R2} capacitively couple the received signal from DAA 120 to the DSP 110. Capacitors C_{C1} and C_{C2} transmit the 20 clock signal and power to the DAA 120. In contrast to the other capacitors in the circuit, which are relatively small (e.g., 5 pF), the charge pump capacitors C_{C1} and C_{C2} are significantly larger (e.g. 100 pF). By increasing the size of the capacitors C_{C1} and C_{C2} , more charge can be transferred per clock cycle and 25 the desirable results described above can be achieved.

The charge pump 132 operates as follows. The driver on the DSP 110 outputs two square wave pulse streams. The two pulse streams are out of phase by 180°. Thus, when the output voltage of capacitor C_{C2} pulses high, the output voltage of capacitor C_{C1} pulses low. During the transition between states current is transferred from C_{C2} to C_{C1} through diode 3. When the voltage output from capacitor C_{C1} pulses high and the voltage output from capacitor C_{C2} pulses low, the charge on capacitor C_{C1} is transferred to VDD through diode D1 and returns through diode D2.

5 Each cycle period of the driver pulse transfers charge to the load across VDD+. The time average current is the average charge per cycle multiplied by 1/T where T is the period of the driver pulse train. The time average current in steady state (when the load across VDD+ is charged up to VDD+) is calculated by the formula $(C_{C2}/T)*2*V_p-3*V_D-V_{DD})$ where V_p is the peak pulse train voltage (325 volts), V_D is the diode forward bias voltage (.7 volts), V_{DD} is the steady state load voltage (approximately 2.7 volts in the preferred embodiment).

10 15

Since current is always available, there is no need to determine the nature of the event before powering up the DAA. This preliminary discrimination step is only required if there is a restriction on the current level. Since the circuitry of the present invention provides this additional power, all signals can be sent directly to the DSP and the DSP can make a decision as to whether or not it wants to process the signal as a real event or disregard the signal as a noise event.

20 25

Alternatively, the present invention could be used with an event discrimination circuit, thereby producing an even more efficient interface because the additional current available would only be used on an as-needed basis, freeing up the added
5 current for use elsewhere.

Having thus described a few particular embodiments of the invention, various alterations, modifications and improvements will readily occur to those skilled in the art. Such alterations, modifications and improvements as are made obvious by this disclosure are intended to be part of this description though not expressly stated herein, and are intended to be within the spirit and scope of the invention. The foregoing description is by way of example only, and not limiting. The invention is limited only as defined in the following claims and equivalents
10
15 thereto.

00192657 00192658

What is claimed is:

1. An interface circuit, comprising:
a digital signal processor (DSP);
a data access arrangement (DAA); and
5 a charge pump, coupled between said DSP and said DAA, said charge pump providing operating power to said DAA.

2. An interface circuit as set forth in claim 1, wherein
said charge pump comprises:

10 a first capacitive element having an input side connected to
said DSP and an output side connected to said DAA;
a second capacitive element having an input and an output
each connected to said DAA; and
a rectifying element coupled between the output side of said
first capacitive element and said second capacitive element.

15 3. An interface circuit as set forth in claim 2, wherein
said DSP includes a clock generator generating first and second
clock pulses out of phase with each other by 180° and wherein
said first capacitive element comprises:

20 a first capacitor coupled to receive said first clock pulse;
and
a second capacitor coupled to receive said second clock
pulse, wherein said first capacitive element continuously outputs
a positive output voltage to said rectifying element.

4. An interface circuit as set forth in claim 3, wherein said rectifying element comprises a diode rectifier.

5. An interface circuit as set forth in claim 4, wherein said DAA includes a clock regeneration element connected in parallel with said rectifying circuit to remove DC level shift and regenerate a clock pulse for use by the DAA which is essentially identical to the clock pulse output by said clock generator.

10 6. An interface circuit as set forth in claim 5, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

15 7. A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

20 inserting a charge pump between said DSP and said DAA; generating a power signal across said charge pump by inputting the output of said clock generator to said charge pump; and

storing said generated power signal for use by said interface.

8. An interface circuit, comprising:
a driver circuit for developing a charge across capacitive
5 elements of said interface circuit;
a data access arrangement (DAA); and
a charge pump, coupled between said DSP and said driver circuit, said charge pump providing operating power to said DAA.

9. An interface circuit as set forth in claim 8, wherein
said charge pump comprises:

a first capacitive element having an input side connected to
said driver circuit and an output side connected to said DAA;
a second capacitive element having an input and an output
each connected to said DAA; and
a rectifying element coupled between the output side of said
15 first capacitive element and said second capacitive element.

10. An interface circuit as set forth in claim 9, wherein
said driver circuit comprises a clock generator generating first
and second clock pulses out of phase with each other by 180° and
20 wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse;
and

a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

11. An interface circuit as set forth in claim 10, wherein
5 said rectifying element comprises a diode rectifier.

12. An interface circuit as set forth in claim 11, wherein
said DAA includes a clock regeneration element connected in
parallel with said rectifying circuit to remove DC level shift
and regenerate a clock pulse for use by the DAA which is
essentially identical to the clock pulse output by said clock
generator.

13. An interface circuit as set forth in claim 12, wherein
said second capacitive element comprises a storage capacitor
which stores the charge transferred by said first and said second
capacitors.

09525674 10 15

ABSTRACT

Disclosed is a method and apparatus which facilitates the use of existing power that is ordinarily unused or discarded to provide power to a telephone interface circuit when the circuit is in the on-hook state, thereby alleviating the need to use loop current to power the interface during the on-hook state. Existing clock signals are used to charge capacitors that are normally used for capacitive coupling of digital data across the high voltage isolation barrier. Although only small-value capacitors are needed for transmitting data across the capacitive interface, larger-value capacitors are used and are configured to form a charge pump to generate power to the interface at all times. Thus the interface always has a steady source of power available for use, including during the on-hook state for powering circuitry that can detect, modulate, and transmit on-hook signals across the capacitive interface.

m:\mds\lucent\22444\specdrft.v02

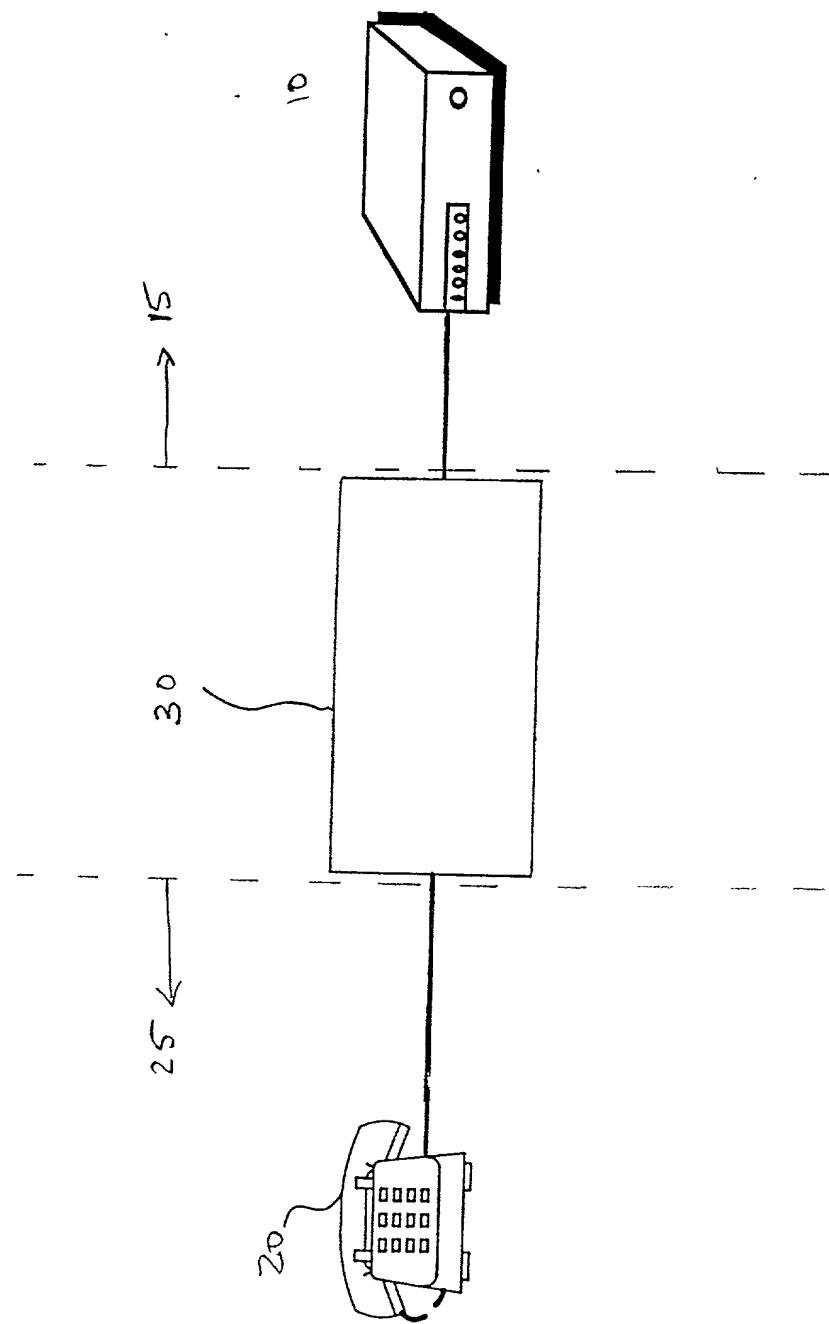
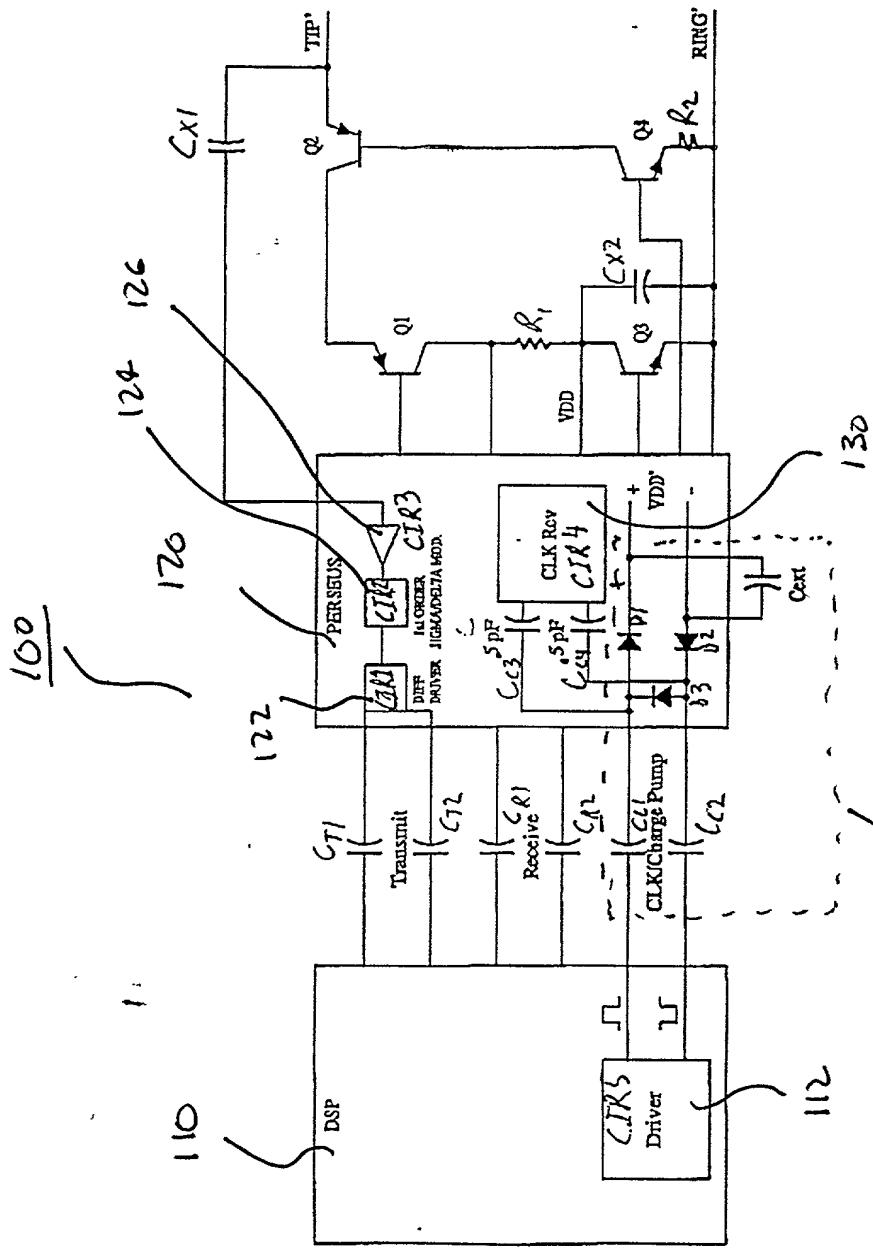


Fig 1



Figs 2

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; and

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Combination Clock and Charge Pump for Line Powered DAA, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of any application on which priority is claimed:

NONE

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NONE

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to

receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

Lester H. Birnbaum	(Reg. No. 25,830)
Richard J. Botos	(Reg. No. 32,016)
Jeffery J. Brosemer	(Reg. No. 36,096)
Kenneth M. Brown	(Reg. No. 37,590)
Donald P. Dinella	(Reg. No. 39,961)
Guy Eriksen	(Reg. No. P-41,736)
Martin I. Finston	(Reg. No. 31,613)
James H. Fox	(Reg. No. 29,379)
Barry H. Freedman	(Reg. No. 26,166)
Julio A Garceran	(Reg. No. 37,138)
Mony R. Ghose	(Reg. No. 38,159)
Jimmy Goo	(Reg. No. 36,528)
Anthony Grillo	(Reg. No. 36,535)
Stephen M. Gurey	(Reg. No. 27,336)
John M. Harman	(Reg. No. 38,173)
Donald E. Hayes, Jr.	(Reg. No. 33,245)
Mark A. Kurisko	(Reg. No. 38,944)
Irene Lager	(Reg. No. 39,260)
Christopher N. Malvone	(Reg. No. 34,866)
Scott W. McLellan	(Reg. No. 30,776)
Martin G. Meder	(Reg. No. 34,674)
Geraldine Monteleone	(Reg. No. 40,097)
John C. Moran	(Reg. No. 30,782)
Michael A. Morra	(Reg. No. 28,975)
Gregory J. Murgia	(Reg. No. 41,209)
Claude R. Narcisse	(Reg. No. 38,979)
Joseph J. Opalach	(Reg. No. 36,229)
Neil R. Ormos	(Reg. No. 35,309)
Eugen E. Pacher	(Reg. No. 29,964)
Jack R. Penrod	(Reg. No. 31,864)
Daniel J. Piotrowski	(Reg. No. P-42,079)
Gregory C. Ranieri	(Reg. No. 29,695)
Scott C. Rittman	(Reg. No. 39,010)
Eugene J. Rosenthal	(Reg. No. 36,658)
Bruce S. Schneider	(Reg. No. 27,949)
Ronald D. Slusky	(Reg. No. 26,585)
David L. Smith	(Reg. No. 30,592)
Patricia A. Verlangieri	(Reg. No. P-42,201)
John P. Veschi	(Reg. No. 39,058)
David Volejnicek	(Reg. No. 29,355)
Charles L. Warren	(Reg. No. 27,407)
Eli Weiss	(Reg. No. 17,765)

I hereby appoint the attorneys on ATTACHMENT A as associate attorneys in the aforementioned application, with full power solely to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected with the prosecution of said application. No other powers are granted to such associate attorneys and such associate attorneys are denied any power or substitution or revocation.

Full Name of First Joint Inventor: **Timothy W. Fuehrer**

Inventor's signature Timothy Fuehrer Date 11/5/98

Residence: **648 Belvidere Road, Phillipsburg, NJ 08865**

Post Office: **648 Belvidere Road, Phillipsburg, NJ 08865**

Citizenship: **USA**

Full Name of Second Joint Inventor: **Keith E. Hollenbach**

Inventor's signature Keith E. Hollenbach Date 11/5/98

Residence: **208 Dickinson Drive, Reading, PA 19605**

Post Office: **208 Dickinson Drive, Reading, PA 19605**

Citizenship: **United States**

Full Name of Third Joint Inventor: **Donald R. Laturell**

Inventor's signature Donald R. Laturell Date 11/5/98

Residence: **10 Highsaddle Lane, Allentown, PA 18104**

Post Office: **10 Highsaddle Lane, Allentown, PA 18104**

Citizenship: **United States**

Full Name of Fourth Joint Inventor: **Steven B. Witmer**

Inventor's signature Steven B. Witmer Date 11/5/98

Residence: **601 Wilshire Blvd., Sinking Spring, PA 19608**

Post Office: **601 Wilshire Blvd., Sinking Spring, PA 19608**

Citizenship: United States

ATTACHMENT A

John T. Synnestvedt	Reg. No. 18,117
Charles H. Lindrooth	Reg. No. 20,659
Irving Newman	Reg. No. 22,638
Alexis Barron	Reg. No. 22,702
Ronald G. Ort	Reg. No. 26,969
Peter J. Butch, III	Reg. No. 32,203
Joseph F. Posillico	Reg. No. 32,290
Mark D. Simpson	Reg. No. 32,942
Theodore Naccarella	Reg. No. 33,023
Patrick J. Kelly, Ph.D.	Reg. No. 34,638
Gary A. Hecht	Reg. No. 36,826
Stephen J. Driscoll	Reg. No. 37,564
Lisa B. Lane	Reg. No. 38,217
Joshua R. Slavitt	Reg. No. 40,816
John A. Chionchio	Reg. No. 40,954
Gregory S. Bernabeo	Reg. No. 44,032
Komlika K. Gill	Reg. No. 43,634

Telephone calls should be made to Synnestvedt & Lechner LLP at:

Telephone: (215) 923-4466
Facsimile: (215) 923-2189

All written communications are to be addressed to:

Mark D. Simpson, Esquire
Synnestvedt & Lechner LLP
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107-2950